REMARKS

Favorable reconsideration of this application, in light of the following discussion and in view of the present amendment, is respectfully requested.

Claims 1 and 13 are amended. Claims 1-9 and 13 are pending.

The Applicants are appreciative of the indication by the Examiner, in the Examiner Interview conducted January 14, 2008, that Zulian does not appear to disclose error detection/correction circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity, and that Watanabe does not appear to disclose that an error detection/correction code generation circuit and an error detection/correction circuit are switched over dependent upon a kind, a length, and a timing of the data to be transferred. Further, in accordance with the Examiner's indication that the application may be placed in condition for allowance if independent claims 1 and 13 were amended to show a purpose or reason as to why the switching over is done, claims 1 and 13 are amended to recite that an error detection/correction code generation circuit and an error detection/correction circuit are switched over in order to detect and correct an error of the data having an error correction code added.

I. Rejection under 35 U.S.C. § 103

In the Office Action, at page 2, numbered paragraph 3, claims 1-5, 7-9 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,701,413 to Zulian in view of U.S. Patent No 5,535,405 to Byers in view of U.S. Patent No. 5,260,951 to Watanabe. This rejection is respectfully traversed because the combination of the teachings of Zulian, Byers and Watanabe does not suggest that each of a plurality of modules includes:

> a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity generating an error correction code to be added to data to be transmitted to the bus connected to the module or to a serial transmission line; and
>
> a plurality of error detection/correction circuits corresponding to a respective one of the error detection/correction code generation circuits, wherein an error detection/correction code generation circuit and an error detection/correction circuit are switched over dependent upon a kind, a length, and a timing of the data to be transferred to detect and correct an error of the data having the error correction code added,

as recited in amended independent claim 1.

Zulian discusses a multi-processor system that includes a plurality of processors 1-4 that are each provided with a memory 5 including a plurality of modules 10-13, 113, 114. Zulian discusses, at col. 4, lines 16-48, cited by the Examiner, that the processors 1-4 are connected together and to a system memory control unit (SMC) 15 by a bus ACBUS 17, and the processors send to the SMC unit 15 requests ABREQ for access to the bus and receive individually a bus grant signal AB GRANT, following which it can effectively occupy the bus 17 and transfer to the SMC unit 15 a memory address and the signals which identify the requested operation such as reading, writing or another type. Zulian further discusses that the unit 15 transfers to the memory 5, via a channel MADDR 18, the read/write address accompanied by suitable timing commands which, in dependence on the address, select and activate one of the various memory modules 10-13, 113, 114. Zulian also discusses at col. 13, lines 43-47, cited by the Examiner, that outputs of multiplexer 56 are connected to the inputs of an 8 bit code generation logic 61 for detection and correction of errors (ECC GEN) and to the inputs of a 72 bit register 62 which also receives on 8 inputs the ECC code generated by the logic 61.

First, Zulian does not discuss or suggest that modules include plural error detection/correction code generation circuits and include plural error detection/correction circuits corresponding to the respective error detection/correction code generation circuits. Zulian discusses only that the system includes controllers 1-4 and a system memory 5, which includes a plurality of modules. The Examiner cites "stations 1-8" as corresponding to a plurality of modules. The controllers are represented in Zulian as elements 1-4, the buffer memory or cache are represented in Zulian as elements 6-9, and the modules are represented in Zulian as modules 10-13, 113 and 114. Thus, it is unclear as to what the Examiner is referring to in discussing stations 1-8. The Examiner appears to be utilizing Byers in alleging that stations 1-8 correspond with the claimed modules.

Further, there is no discussion or suggestion in Zulian that either the processors 1-4 or the modules 10-13, 113 and 114 include error detection/correction code generation circuits and error detection/correction circuits corresponding to a respective one of the error detection/correction code generation circuits. Zulian discusses only detection and correction of errors, but Zulian does not suggest that the modules 10-13, 113 or 114 include error detection/correction code generation circuits or circuits corresponding to the error detection/correction code generation circuits. In addition, at col. 4, lines 16-48 and col. 13, lines 43-47, Zulian does not suggest that error detection/correction code generation circuits or circuits corresponding to the generation circuits are provided in each of the modules 10-13, 113 and 114.

In addition, Zulian does not discuss or suggest, and the Office Action fails to address that the modules 10-13, 113, 114 have error detection/correction code generation circuits that have a difference in at least one of an inspection bit length, an information bit length, and a correction capacity. Col. 4, lines 16-48 of Zulian discuss only that the processors 1-4 send to the SMC unit 15 requests ABREQ for access to the bus and receive individually a bus grant signal AB GRANT, following which it can effectively occupy the bus 17 and transfer to the SMC unit 15 a memory address and the signals which identify the requested operation such as reading, writing or another type. Zulian does not discuss that multiple error detection/correction code generation circuits exist which have differences between, for example, information bit lengths.

In contrast, the present specification discusses that, for example, detection/correction circuit #B detects and corrects an error of data of single 32 bits and detection/correction circuit #C detects and corrects an error of data of single 64 bits of a double data width. Thus, as recited in independent claim 1, for example, the present invention includes error detection/correction code generation circuits that differ depending on, for example, information bit length, correction capacity, etc. Zulian includes no distinction between multiple error detection/correction circuits, based on inspection or information bit length, or correction capacity.

In addition, Zulian does not discuss or suggest that error detection/correction code generation circuits generate an error correction code to be added to data to be transmitted to the bus connected to a module or to a serial transmission line. Zulian does not suggesting adding an error correction code to data.

The Examiner indicates that Byers make up for some of the deficiencies in Zulian. The Applicants respectfully disagree.

Byers discusses a bus controller system in which stations 1-8 are connected to a bus. Byers does not make up for the deficiencies in Zulian. The Examiner alleges that "it would have been obvious to a person of ordinary skill in the art at the time of the invention to improve upon the multi-processor computer system, as disclosed by Byers. Doing so would efficiently control the operation of special purpose gate arrays intended to store and transfer data between a special purpose gate array and an external device or system and between special purpose gate arrays." It is entirely unclear as to how controlling the operation of special purpose gate arrays would have led one of ordinary skill in the art to suggest incorporating the stations 1-8, which are connected to bus 218 of Byers, into the system of Zulian, to suggest that modules connected via buses in a controller include error detection/correction code generation circuits and error detection/correction circuits corresponding to the error detection/correction code generation

circuits. It is unclear as to how controlling gate array operation is an apparent reason or motivation which would have led one of ordinary skill in the art to combine the teachings of Zulian and Byers to suggest the modules of claim 1, for example.

Further, as conceded by the Examiner, Zulian does not also suggest that an error detection/correction code generation circuit and an error detection/correction circuit are switched over dependent upon a kind, a length, and a timing of the data to be transferred. In addition, Zulian does not suggest does an error detection/correction code generation circuit and an error detection/correction circuit are switched over in order to detect and correct an error of the data having the error correction code added.

The Examiner indicates that Watanabe make up for the deficiencies in Zulian and Byers. The Applicants respectfully disagree.

Watanabe does discuss an error correction circuit, but Watanabe does not discuss or suggest that an error detection/correction code generation circuit and an error detection/correction circuit corresponding to the error detection/correction code generation circuit are switched over dependent upon a kind, a length, and a timing of the data to be transferred. The Examiner alleges that Watanabe discusses such at col. 1, line 62 – col. 2, line 14. The Applicants respectfully disagree.

Col. 1, line 62 – col. 2, line 14 of Watanabe discusses a system for detecting and distinguishing proper decoding of a signal when a plurality of error correction encoding and decoding methods are executed depending on characteristics of different signals. Watanabe further discusses that consecutive data frames are transmitted and received by Time Division in a selected channel and a plurality of data respectively inserted into a frame is encoded by a plurality of encoding methods for error corrections depending on characteristics of the data.

While Watanabe does discuss error corrections and encoding/decoding for error corrections depending on characteristics of the data, Watanabe does not discuss or suggest that an error detection/correction code generation circuit and an error detection/correction circuit corresponding to the error detection/correction code generation circuit are switched over depending on the type of data to be transferred. Watanabe does not suggest that an error detection/correction code generation circuits and an error detection/correction circuit, of multiple error detection correction code generation circuits and multiple error detection/correction circuits, are switched over based on the characteristics of the data. Watanabe discusses only that data are encoded by a plurality of encoding methods for error corrections depending on the

characteristics of the data, but does not suggest that error detection/correction circuits are switched over dependent on the characteristics of the data.

Further, Watanabe does not suggest that the error detection/correction circuits are switched over dependent on a kind, a length, **and** a timing of the data to be transferred. Watanabe discusses only that the distinction between characteristics of data is the distinction between a voice signal and a control signal, for example. Watanabe does not, however, suggest that characteristics of data as to a kind, a length and a timing of the data to be transferred are used to switch over error detection/correction circuits.

Also, Watanabe does not suggest that the circuits are switched over in order to detect and correct an error of the data having the error correction code added. As Watanabe does not discuss switching over circuits, Watanabe is also not suggestive of doing so for the purpose of detecting and correcting an error of the data having the error correction code added.

In addition, the Examiner alleges that "it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Zulian with the decoding system, as disclosed by Kikuchi (assumed to refer to Watanabe). Doing so would improve an improved system for data communication in which digital data can be properly reconverted." The Applicants respectfully disagree.

It is entirely unclear as to how properly reconverting digital data is an apparent reason or motivation to have led one of ordinary skill in the art to combine the error correction encoding/decoding methods executed depending on characteristics of different signals of Watanabe with the system of Zulian, which does not discuss or suggest error detection/correction circuits, to suggest switching over error detection/correction circuits dependent on a kind, a length, and a timing of the data to be transferred.

Therefore, as the combination of the teachings of Zulian, Byers and Watanabe does not suggest that each of a plurality of modules includes "a plurality of error detection/correction code generation circuits having a difference in at least one of an inspection bit length, an information bit length, and a correction capacity generating an error correction code to be added to data to be transmitted to the bus connected to the module or to a serial transmission line; and a plurality of error detection/correction circuits corresponding to a respective one of the error detection/correction code generation circuits, wherein an error detection/correction code generation circuit and an error detection/correction circuit are switched over dependent upon a kind, a length, and a timing of the data to be transferred to detect and correct an error of the data having the error correction code added," as recited in amended independent claim 1, and as the

motivations cited by the Examiner are inadequate to suggest combining the references, claim 1 patentably distinguishes over the references relied upon. Accordingly, withdrawal of the §103(a) rejection is respectfully requested.

Further, the combination of the teachings of Zulian, Byers and Watanabe does not suggest "a plurality of modules connected via buses to transmit data, each of the modules including, a plurality of error detection/correction code generation circuits and a plurality of error detection/correction circuits corresponding to a respective one of the error detection/correction code generation circuits, the plurality of error detection/correction code generation circuits generating an error correction code to be added to the data to be transmitted to one of the buses connected to one of the modules, wherein an error detection/correction code generation circuit and an error detection/correction circuit are switched over dependent upon a kind, a length, and a timing of the data to be transferred to detect and correct an error of the data having the error correction code added," as recited in amended independent claim 13, and the motivations cited by the Examiner are inadequate to suggest combining the references. Therefore, claim 13 patentably distinguishes over the references relied upon. Accordingly, withdrawal of the §103(a) rejection is respectfully requested.

Claims 2-9 depend either directly or indirectly from independent claim 1 and include all the features of claim 1, plus additional features that are not discussed or suggested by the references relied upon. For example, claim 3 recites that "the error detection/correction system switches over error detection/correction codes to be used dependent upon whether at a time of single access or at a time of burst access." The Examiner cites col. 17, lines 49 through col. 18, line __ of Watanabe to suggest that Watanabe discusses such. The Watanabe reference has only 6 columns. Therefore, it is unclear as to where in Watanabe the Examiner alleges that Watanabe discloses, for example, that an error detection/correction system switches over error detection/correction codes to be used dependent upon whether at a time of single access or at a time of burst access. Watanabe does not suggest such. Therefore, claims 2-9 patentably distinguish over the references relied upon for at least the reasons discussed above. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

II. Allowable Subject Matter

Applicants are appreciative of the indication that claim 6, which is objected to as being dependent upon a rejected base claim, would be allowable if rewritten in independent form. As claim 1, from which claim 6 ultimately depends, is believed to be allowable over the references relied upon, claim 6 has not been rewritten in independent form.

Conclusion

In accordance with the foregoing, claims 1 and 13 have been amended. Claims 1-9 and 13 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 1/20/08

By: _____

Kari P. Footland
Registration No. 55,187

1201 New York Avenue, N.W., 7th Floor
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501